ABSTRACT OF THE DISCLOSURE

First and second vertical structures are formed on first and second surface regions of a silicon substrate. Each of the first and second vertical structures includes a tunneling layer pattern, a charge trapping layer pattern, and blocking layer pattern sequentially stacked on the silicon substrate. A gate insulating layer is formed on a third surface region of the silicon substrate which is interposed between the first and second surface regions of the silicon substrate. First and second gate spacers are formed on respective surface portions of the gate insulating layer, with the first gate spacer contacting an upper portion of a sidewall of the first vertical structure and protruding above an upper surface of the first vertical structure, and the second gate spacer contacting an upper portion of a sidewall of the second vertical structure and protruding above an upper surface of the second vertical structure. A gate forming conductive layer is formed on exposed surfaces of the first and second vertical structures, the first and second gate spacers, and the gate insulating layer, and the gate forming conductive layer is then etched to form first and second gate electrodes, where the first and second gate electrodes expose portions of the first and second vertical structures and the gate insulating layer. Portions of the first and second vertical structures and the gate insulating layer exposed by the first and second gate electrodes are removed by performing an etching process using the first and second gate electrodes as an etch mask. A source region and a drain region are then formed by implanting impurity ions in portions of the silicon substrate exposed by the first and second gate electrodes.